

**ESD PROTECTION DEVICE AND CIRCUIT DESIGN FOR  
ADVANCED CMOS TECHNOLOGIES**

**Yvonne Gersten**

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Figure Typical failure threshold current of ESD protection devices . protection circuits designed for one generation of the technology may not be suitable for the . However, in the advanced CMOS processes, the breakdown voltage of the.

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It turns out that the distributed network shown in Figure 4 offers significant advantages in ESD performance and design flexibility. Unfortunately, this does not guarantee improved performance.

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this is somewhat unrealistic for actual chip stressing, it was the most useful for network optimization purposes because it provides the highest stress across the fragile NMOS output buffer.